

REMARKS

Claims 1-23 are pending in the above-identified application. Claims 12-23 are withdrawn. Claims 1, 3, 6, 8, and 10 are cancelled. Claims 2, 5, and 7 are amended. No new subject matter is added. It is respectfully submitted that this Amendment is fully responsive to the Office Action dated August 23, 2005.

Claims 1, 2, 6 and 7 were objected to because of informalities. Claims 1 and 6 are cancelled. Claims 2 and 7 are amended so as to clarify that the “high” dielectric constant film has a higher dielectric constant than silicon oxide film. These amendments to claims are based on the descriptions of the specification on, for example, page 2, lines 8-11 and page 30, lines 6-9. Accordingly, Applicants respectfully request that the Examiner withdraw the objections to these claims.

Claims 1 and 6 were rejected under 35 U.S.C. §102(b) as being anticipated by *Rodder et al.* (US 6,251,761). Claims 1 and 6 are cancelled. Accordingly, this rejection is now moot.

Claims 2-7 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Watanabe* (U.S. Pat. No. Pub 20050167761) in view of *Chau et al.* (U.S. Pat. No. 6,713,358). Claims 3 and 6 are cancelled and claims 2, 5, and 7 are amended. In view of these amendments and the following remarks, Applicants respectfully request that the Examiner withdraw the rejection of these claims.

Watanabe discloses two transistors which have gate insulation films of different multilayered structure, one having a gate insulation film formed of a silicon oxidation film (403)

formed on the silicon substrate (401), ZrO₂ film (404) formed on the oxidation film (403) and Zr silicate film (405) formed on the ZrO₂ film (404), the other having a gate insulation formed of a silicon oxidation film (403) formed on the silicon substrate (401) and ZrO₂ film (404) formed on the oxidation film (403) (FIGs. 4A-4D). The two gate insulation films of different multilayered structure in FIGs. 4A-4D commonly include the silicon oxidation films (403). In FIGs. 5A-5D and FIGs. 6A-6D of *Watanabe*, two gate insulation films of different multilayered structure commonly include silicon oxidation films (503) or SiON film (603).

The present invention according to claim 2 has the structural feature that the first gate insulation film includes the silicon oxide-based insulation film formed on the semiconductor substrate, the high dielectric constant film formed on the silicon oxide-based insulation film and the oxygen diffusion preventing film formed on the high dielectric constant, while the second gate insulation includes the high dielectric constant film formed directly on the semiconductor substrate and the oxygen diffusion preventing film formed on the high dielectric constant film. Namely, the first insulation film includes the silicon oxide-based insulation film between the substrate and the high dielectric constant film, while the silicon oxide-based insulation film is removed before forming the high dielectric constant film in the second insulation film. Thus, there is a structural difference regarding the set of gate insulation films between the present invention according to claim 2 and *Watanabe*, as the second gate insulation includes the high dielectric constant film formed directly on the semiconductor substrate in the present invention according to claim 2.

In the present invention according to claim 2, the first gate insulation film for the first transistor including the first gate electrode as a high voltage resistant transistor includes the silicon oxide-based insulation film, while the second gate insulation film for the second transistor including the second gate electrode as a low voltage operative transistor includes the high dielectric constant film formed directly on the semiconductor substrate, whereby gate leak current in the high voltage resistant transistor can surely suppressed to ensure high reliability, keeping the performance of the low voltage operative transistor high.

As described above, the present invention according to claim 2 is different from *Watanabe* in the point that the first gate insulation film includes the silicon oxide-based insulation film while the second gate insulation film includes the high dielectric constant film formed directly on the semiconductor substrate. Therefore, even if *Chau et al.* teaches the oxygen diffusion preventing film formed on the high dielectric constant film, the combined teachings of *Watanabe* and *Chau et al.* do not teach or suggest the present invention according to claim 2. Accordingly, it is clear that the present invention according to claim 2 would not have been obvious to one of ordinary skill in the art at the time the invention was made.

The present invention according to claim 7 also has the structural feature that the first gate insulation film includes a silicon oxide-based insulation film formed on the semiconductor substrate and the reduction-retardant high dielectric constant film formed on the silicon oxide-based insulation film, while the second gate insulation film includes the high dielectric constant film formed directly on the semiconductor substrate. Namely, the first insulation film includes

the silicon oxide-based insulation film between the substrate and the high reduction-retardant dielectric constant film, while the silicon oxide-based insulation film is removed before forming the reduction-retardant high dielectric constant film in the second insulation film.

As discussed regarding claim 2, the present invention according to claim 7 is also different from *Watanabe* in the manner of the formation of the silicon oxide-based insulation film and the combined teachings of *Watanabe* and *Chau et al.* do not teach or suggest the present invention according to claim 7. Accordingly, it is clear that the present invention according to claim 7 would have been obvious to one of ordinary skill in the art at the time the invention was made.

Moreover, as described above, even if *Watanabe* was combined with *Chau et al.* it is clear that the present invention according to claim 2 would not have been obvious to one of ordinary skill in the art at the time the invention was made. Therefore, it is also clear that the present invention according to claims 4 and 5 dependent from claim 2 would not have been obvious to one of ordinary skill in the art at the time the invention was made.

Claims 8-11 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Watanabe* further in view of *Chau et al.* and further in view of *Yu et al.* (U.S. Pat. No. 6,784,101). Claims 8 and 10 are cancelled. In view of this and the following remarks, Applicants respectfully request that the Examiner withdraw the rejection of these claims.

Amendment Under 37 C.F.R. §1.111

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As described above, even if *Watanabe* was combined with *Chau et al.* it is clear that the present invention according to claim 7 would have been unobvious to one of ordinary skill in the art at the time the invention was made. Therefore, even if *Watanabe* and *Chau et al.* were further combined with *Yu et al.*, which only discloses the usage of the hafnium aluminates film as a high dielectric film, it is clear that the present invention according to claims 9 and 11 dependent from claim 7 would not have been obvious to one of ordinary skill in the art at the time the invention was made.

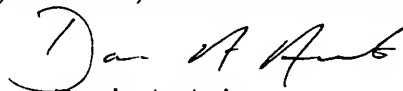
For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone applicants' undersigned attorney.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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